flash memory cell for storing data at the flash memory cell ~~claimed in claim 11~~ according to the present invention is characterized in that if electrons are to be injected into the first floating gate, a programming operation is performed by applying a programming voltage to the control gate, connecting the first junction region and the ground terminal and applying a voltage lower than the programming voltage but higher than the ground voltage to the second junction region, and if the electrons are to be injected into the second floating gate, the programming operation is performed by applying a programming voltage to the control gate, applying a voltage lower than the programming voltage but higher than the ground voltage to the first junction region and connecting the second junction region and the ground terminal, wherein the programming operations are independently performed for the first floating gate and the second floating gate.

In a still another preferred embodiment, the erasing method of the flash memory cell for erasing data stored at the flash memory cell ~~claimed in claim 11~~ according to the present invention is characterized in that if electrons injected into the first floating gate are to be discharged, an erasing operation is performed by applying an erasing voltage to the control gate, and applying a voltage higher than the ground voltage to the second junction region with the first junction region floated, and if electrons injected into the second floating gate are to be discharged, the erasing operation is performed by applying the erasing voltage to the control gate, and applying a voltage higher than the ground voltage to the first junction region with the second junction region floated, wherein the erasing operations are independently performed for the

first floating gate and the second floating gate.

In a still another preferred embodiment, the reading method of a flash memory cell for reading data stored at the flash memory cell ~~claimed in claim 11~~ according to the present invention is characterized in that a reading operation is performed by applying a reading voltage to the control gate, connecting the first junction region to the ground terminal, applying a voltage lower than the reading voltage but higher than the ground voltage to the second junction region and then sensing cell current flowing into the second junction region, or by applying the reading voltage to the control gate, connecting the second junction region to the ground terminal, applying a voltage lower than the reading voltage but higher the ground voltage to the first junction region, and then sensing cell current flowing into the first junction region.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

In another aspect of the present invention, it is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.